Remarks/Arguments

In the non-final Office Action mailed on 25 March 2004, the Examiner rejected all claims 1-20 under 35 U.S.C. §102(e) as anticipated by Thekkath (United States Patent Number 6,393,500). Applicant respectfully traverses the rejection. Applicant has amended claims 1, 6, 11 and 16 for editorial clarity and to better protect the invention. Applicant respectfully requests reconsideration and withdrawal of the outstanding rejection.

Withdrawn Restriction Requirement

On 15 December 2003, the Examiner issued a restriction requirement identifying group 1 as claims 1-10 and group 2 as claims 11-20. On 12 January 2004, Applicant responded to the restriction requirement by traversing and provisionally electing group 1 claims. No further comment or action was received from the Examiner until this Office Action mailed 25 March 2004. This Office Action addresses the merits of all claims 1-20 as though no election was made but does not clearly state that the restriction requirement was withdrawn. In a telephone conference with the Examiner on 22 June 2004, the undersigned attorney clarified the Examiner's intent to withdraw the restriction requirement thereby leaving all 20 claims pending in the subject application.

§102 Rejection

The Examiner rejected all claims 1-20 under 35 U.S.C. §102(e) as anticipated by Thekkath. In particular, as regards rejected claim 1, the Examiner suggests that Thekkath teaches the recited bus bridge device as burst-configurable bus master 610 of Thekkath's figure 6 or as peripheral interface logic 120 of figure 1. The Examiner then suggests that the recited detector element of claim 1 reads on the same bus master 610 and cites column 13, lines 24-25 in support of the function of detecting a burst transaction having an indefinite length. Lastly, the Examiner suggests that the recited translator element reads on transaction control element 616 of Thicket's figure 6 and cites column 13, lines 51-56 and element 712 of figure 7 in support therefore.

Applicant strongly disagrees with the Examiner's reading of the rejected claim elements on the teachings of Thekkath.

First, neither peripheral interface logic 120 of Thicket's figure 1 nor bus master 610 of figure 6 are a bus bridge device as recited in the rejected claim. The recited bus bridge device is coupled to a first bus and to a second bus and includes a detector for detecting a burst transaction ***on the first bus*** and a translator for generating and applying a translated burst transaction ***to the second bus***. Neither peripheral interface logic 120 nor bus master 610 of Thekkath teach or reasonably suggest such a coupling to two buses to detect and translate indefinite burst transactions from a first bus for application to a second bus.

Peripheral interface logic 120 of Thicket's figure 1 may be reasonably understood as a bridge device as the term is broadly defined in the subject application in that it forwards transactions from system bus 112 to slower devices on peripheral interface bus 122. However, nothing in Thekkath suggests that bus 122 permits any form of burst transactions. Thekkath is simply silent as to the types of bus transaction that may be applied to bus 122. To the contrary, the fact that bus 122 is used for "slower devices" suggests precisely the opposite – that the peripheral interface bus would not have need for high speed burst transactions. Thekkath is silent as to the characteristics of the peripheral interface bus since it has nothing to do with the nature of his invention. Rather, Thekkath teaches a logic structure that may be integrated into or with a bus master device to permit a bus master device to customize the burst transaction it issues for the burst characteristics of the slave device. The nature of bus transactions between the peripheral interface logic 120 and the devices on the peripheral interface bus 122 are irrelevant to the bus master burst generation logic to which Thekkath is addressed. Hence, there is no teaching in Thekkath of a detector or translator to detect and translate an indefinite length burst transaction from a first bus for application to a second bus as a new burst transaction. Further, such a feature is clearly not inherent in all "bus bridge" structures. Therefore, peripheral interface logic 120 does not teach or reasonably suggest the recited bus bridge device of rejected claim 1.

Bus master 610 of Thicket's figure 6 likewise teaches nothing of the recited bus bridge device of rejected claim 1. Rather, bus master 610 exemplifies an enhanced bus master device in accordance with teachings of Thekkath wherein burst transactions applied to the data bus 630 may be customized in width and length for each intended target slave device. Thicket's bus master 610 is not coupled to a first and second bus as is the recited bus bridge of rejected claim 1. Bus master 610 is coupled to two distinct buses – address bus 620 and data bus 630. However, the address bus does not perform burst transactions – it is not a first bus as recited on which indefinite length burst transactions are detected. Rather, the address bus 620 provides the addressing information to identify a target slave device so that burst parameters of the slave may be determined. Once the burst characteristics of the identified slave device are determined, a burst transaction may be customized by the bus master 610 for transfer of data over the data bus 630 to the intended slave device. Hence, there is no detection of an indefinite length burst transaction on a first bus as recited in the rejected claim nor is there translation of that detected burst transaction to generate a new burst transaction having a predetermined length. Thekkath teaches the customized generation of but a single data burst transaction applied to a single bus – the data bus 630. See, e.g., Thekkath column 13, line 34 through column 14, line 7. Thekkath does not teach or suggest that there are burst transactions detected on a first bus (presumably read by the Examiner as address bus 620) nor that such a detected burst transaction is translated to a new burst transaction for application to the second bus (presumably the data bus 630). Rather, as noted, Thekkath teaches customized generation of a single burst transaction for application to the data bus 630.

Still further, it would be nonsensical to suggest burst transactions on an address bus 620 as shown in Thekkath. An address bus (as distinct from a separate data bus as taught by Thekkath) would have no use for burst transactions. The volume of information exchanged over an address bus is by its nature minimal – arbitration and address information is typically exchanged. Burst transactions are useful for rapid, low overhead transfer of large volumes of data as is transmitted over the data bus 630 – not a single address and arbitration information as is typically exchanged over the address bus 620.

Second, nothing in Thekkath teaches or reasonably suggests that the detected burst transactions are of indefinite length as recited in rejected claim 1. The rejected claim recites that the detected burst transaction has an "indefinite length." The clear meaning of "indefinite" as used consistently throughout the subject application is a burst transaction having no predetermined, fixed length. As recited in the specification of the subject application, other bus signals are sometimes used to determine the completion of such an indefinite burst transaction. See, e.g., page 2of the subject application at lines 5-6.

Further, the translation element of the claimed bus bridge translates such an indefinite length burst transaction (detected on the first bus) into a new burst transaction having a predetermined length for application to the second bus coupled to the bridge. No such translation is taught or suggested by Thekkath. Rather, all burst transactions in Thekkath have a fixed determinable length. The Examiner points to column 13, lines 24-25 as supporting a teaching of indefinite length burst transactions. The cited passage refers to "variable" burst length, not indefinite burst length. All burst transactions taught by Thekkath have a determined length – the total length of the burst. The length and width of the customized burst transaction may be varied in Thekkath according to the needs of a particular slave device but the total length of the burst transaction is known and hence predetermined. Thekkath teaches varying the burst width (in bits/bytes) and varying the length (in cycles) but the total length of the burst is predetermined – not indefinite. Thekkath provide examples of such variable width and length in figures 8 and 9. Both exemplary transfers in Thekkath transfer 32 bytes of data – the predetermined fixed total length of the burst transaction. In figure 8, the burst transaction width is 32 bits and hence the total transfer required 8 data transfer cycles (i.e., a burst length of 8). The burst transfer of figure 9 also transfers 32 bytes but uses a 64 bit width and hence a burst length of 4 cycles. The total transfer length of 32 bytes in both exemplary burst transfers is known in advance and hence predetermined – not indefinite as recited in rejected claim 1. Thicket's teaching of variable width and length therefore does not teach or suggest the indefinite length recitation of rejected claim 1.

For at least the above reasons, claim 1 is not anticipated by the teachings of Thekkath. Further, the claimed features are neither taught nor reasonably suggested by any art of record, considered individually or in any combination. Applicant therefore maintains that rejected claim 1 is allowable over all art of record.

Independent claim 6 was rejected for similar reasons and recites a related method claim useful in a bus bridge such as claimed in claim 1. For similar reasons to those discussed above, Applicant maintains that claim 6 is allowable over all prior art of record, considered individually or in any combination.

Independent claims 11 and 16 are similar to claims 1 and 6, respectively, and were rejected for similar reasons. Claims 11 and 16 differ from claims 1 and 6, respectively, in that each recites a slave device as distinct from a bus bridge device and a related method of operation therefore. For similar reasons to those presented above, Applicant maintains that claims 11 and 16 are allowable over all prior art of record, considered individually or in any combination.

Dependent claims 2-5, 7-10, 12-15 and 17-20 depend from base claims 1, 6, 11 and 16, respectively. For at least the same reasons as discussed above and as dependent upon allowable base claims, Applicant maintains that dependent claims 2-5, 7-10, 12-15 and 17-20 are allowable over all art of record, considered individually or in any combination.

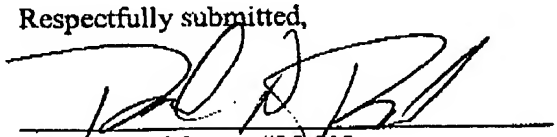
Applicant therefore respectfully requests reconsideration and withdrawal of the rejection of all claims 1-20.

Conclusion

Applicant has amended claims 1, 6, 11 and 16 for editorial clarity and to better protect the invention. Applicant has thoroughly discussed the rejection under §102. Applicant has respectfully requested reconsideration and withdrawal of the outstanding rejection.

No additional fees are believed due. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

Respectfully submitted,



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